APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PROCESSOR RESET

Abstract of the Invention

When a RESET signal is generated in a target processor during a test procedure, a reset sync marker is generated in a program counter trace stream. The reset sync marker includes a plurality of packets, the packets identifying that the reset sync marker is the result of a RESET signal. The packets identify the program counter address at the time of the generation of the RESET signal and relate the reset sync marker to a timing trace stream. When the RESET signal is removed, a second (reset-off) sync marker is generated identifying the removal of the RESET signal, identifying the program counter address, and relating the second sync marker to the timing trance stream.